

PRELIMINARY INFORMATION

AD9853

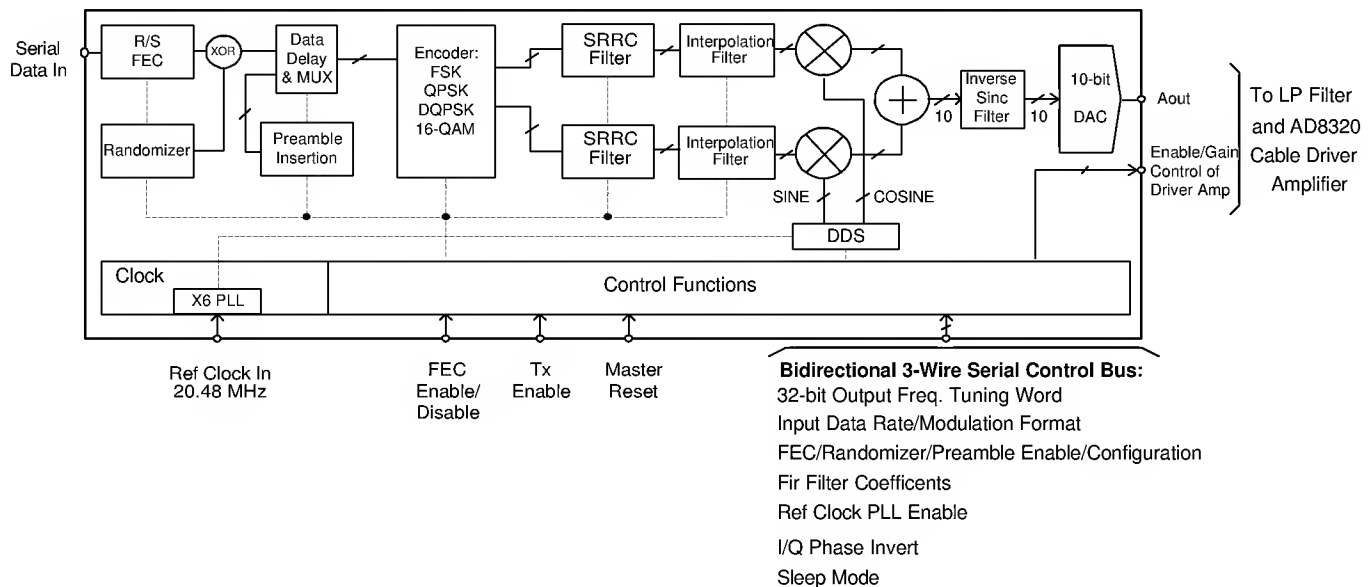
FEATURES

Universal Low-cost Solution for HFC Network
 Return-channel Tx Function: 5-40 MHz/5-65 MHz
 Includes Programmable SRRC Pulse-shaping Filter and
 Programmable Input Data Rates
 QPSK/DQPSK/16-QAM Input Data Format
 Internal Reference Clock Multiplier
 R/S FEC Function w/on-the-fly enable/disable control
 Programmable Randomizer/Preamble Function
 Supports Inter-operable Cable Modem Standards
 Internal SINX/X Compensation

>50dB SFDR @ 42 MHz Output Frequency
 Controlled Burst Mode Operation
 +3.3V or +5 V Single Supply Operation
 Low Power: 600 mW@ Full Clock Speed (3.3 V supply)
 Space-saving Surface-mount Packaging
 Bi-directional Control Bus Interface

APPLICATIONS

HFC Data, Telephony, and Video Modems



FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD9853 integrates a high-speed direct-digital synthesizer (DDS), a high-performance, high-speed digital-to-analog converter (DAC), digital filters, and other DSP functions onto a single chip, to form a complete digital modulator device. The AD9853 is intended to function as the upstream modulator in interactive HFC cable network applications, where cost, size, power dissipation, functional integration, and dynamic performance are critical attributes.

The AD9853 is fabricated on an advanced CMOS process and it sets a new standard for CMOS digital modulator

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performance. The device is loaded with application-specific functionality and provides a direct interface port to the AD8320, digitally-programmable cable driver amplifier. The AD9853/AD8320 chipset forms a highly-integrated, low-power, small footprint, and cost-effective solution for the inter-operable HFC return-path requirement.

The AD9853 is available in a space-saving surface mount package and is specified to operate over the extended industrial temperature range of -40° to +85°C. result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

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ABSOLUTE MAXIMUM RATINGS¹

Maximum Junction Temp.	+165°C	Storage Temperature	-65°C to +150°C
Vs	+6V	Operating Temp.	-40°C to +85°C
Digital Inputs	-0.7V to +Vs	Lead Temp. (10 sec. soldering)	+300°C
Digital Output Current	5mA		

AD9853 ELECTRICAL CHARACTERISTICS (Vs=+3.3 V ±5%, Rset=3.9 k Ω, Reference Clock Frequency = 20.48 MHz with internal clock multiplier enabled).

Parameter	Temp	Test Level	AD9853			Units
			Min	Typ	Max	
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
CLK Multiplier Disabled	FULL	VI			170.0	MHz
CLK Multiplier Enabled	FULL	VI			28.3	MHz
Duty Cycle	+25°C	I		50		%
Input Capacitance	+25°C	IV		3		pF
Input Impedance	+25°C	IV		100		MΩ
DAC OUTPUT CHARACTERISTICS						
Resolution				10		Bits
Full Scale Output Current	+25°C	V		10	20	mA
Full Scale Output V into 37.5Ω Load ²	+25°C	V	4I			dBmV
Gain Error	+25°C	I		TBD		%FS
Output Gain Flatness (DC to Nyquist)	+25°C	I		± .05		dB
Output Offset	+25°C	I		TBD		uA
Differential Non-linearity	+25°C	I		.5		lsb
Integral Non-linearity	+25°C	I		1		lsb
Output Slew Rate	+25°C	IV		TBD		V/nS
Output Capacitance	+25°C	I		5		pF
Phase Noise @ 1 kHz Offset, 40 MHz Aout ³	+25°C	I		-100		dBc
Voltage Compliance Range	+25°C	I	0		1.5	V
Wideband SFDR:						
1 MHz Analog Out	+25°C	V		65		dBc
20 MHz Analog Out	+25°C	V		60		dBc
42 MHz Analog Out	+25°C	V	48	50		dBc
65 MHz Analog Out ⁴	+25°C	V	45	48		dBc
>65 MHz Analog Out ⁵	+25°C	V	46			dBc
Feedthrough with Device Off	+25°C	V			+5	dBmV
MODULATOR CHARACTERISTICS						
Modulator Carrier Suppression	+25°C	I	35			dB
I/Q Amplitude Imbalance	+25°C	I			0.5	dB
Total Implementation Loss						
QPSK Mode	+25°C	IV			0.5	dB
16-QAM Mode	+25°C	IV			0.75	dB
Error Vector Magnitude	+25°C	I		3		%
I/Q Phase Imbalance	+25°C	I			1	Deg.
Pass Band Amplitude Ripple	+25°C	I	-0.3		+0.3	dB
TIMING CHARACTERISTICS						
t _{wh} , t _{wl} (W_CLK min. pulse width high/low)	+25°C	IV	TBD			ns
t _{ds} , t _{dh} (Data to W_CLK setup and hold times)	+25°C	IV	TBD			ns
t _{fs} , t _{fn} (FQ_UD to REF CLK setup and hold times)	+25°C	IV	TBD			ns
t _{ns} , t _{nl} (FQ_UD min. pulse width high/low)	+25°C	IV	TBD			ns
t _{rs} (RESET minimum pulse width)	+25°C	IV	TBD			ns
t _{sr} (RESET to REF CLK setup time)	+25°C	IV	TBD			ns
t _{fd} (FQ_UD min. delay after W_CLK)	+25°C	IV	TBD			ns
Normal Mode Data latency					TBD	Symbols
Burst Mode Data Latency					TBD	Symbols

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AD9853 ELECTRICAL CHARACTERISTICS (Vs=+3.3V±5%, Rset=3.9 k Ω, Reference Clock Frequency = 20.48 MHz with clock multiplier enabled).

Parameter	Temp	Test Level	AD9853			Units
			Min	Typ	Max	
CMOS LOGIC INPUTS						
Logic "1" Voltage	+25°C	I	+2.7			V
Logic "0" Voltage	+25°C	I				+0.4 V
Logic "1" Current	+25°C	IV				12 uA
Logic "0" Current	+25°C	IV				12 uA
Input Capacitance	+25°C	V	3			pF
POWER SUPPLY						
+Vs Current @ Full Operating Conditions	+25°C	I	181			mA
P _{DISS} @ Full Operating Conditions	+25°C	I	600			mW
P _{DISS} @ Power-down Mode	+25°C	I	10			mW

NOTES

¹ Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

²DC to 42 MHz output bandwidth.

³Residual phase noise

⁴Reference clock=27 MHz with clock multiplier enabled; supply voltage=+ 5V

⁵Excluding aliased frequency components

EXPLANATION OF TEST LEVELS

Test Level

- I - 100% Production Tested.
- III - Sample Tested Only.
- IV - Parameter is guaranteed by design and characterization testing.
- V - Parameter is a typical value only.
- VI - All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

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Table I. MODULATOR FUNCTION DESCRIPTION

Data Format	FSK*, QPSK, DQPSK, differential 16-QAM, selectable via control bus
Output Carrier Frequency Range	5-42 MHz with 20.48 MHz reference clock (+3.3 V supply voltage) 5-65 MHz with 27.792 MHz reference clock (+5 V supply voltage)
Differential Encoder	Enable/disable control via control bus
Input Data Rate	120 kb/s - 10 Mb/s programmable via control bus
Symbol rate	
Pulse-shaping Filter	41 Tap, 10-bits each, fully-programmable coefficients via control bus
Reference Clock Frequency	(5-40 MHz Aout) 20.48 MHz w/PLL enabled, 122.88 MHz w/PLL disabled (5-65 MHz Aout) 27.792 MHz w/PLL enabled, 166.752 MHz w/PLL disabled
Internal Reference Clock Multiplier	Fixed X6, enable/disable control via control bus
Data Oversample Rate	4X
R/S FEC	Dedicated Enable/disable control pin as well as enable/disable via control bus Selectable via control bus: Field generator polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$ Code generator polynomial: $g(x) = (x + \alpha^0)(x + \alpha^1)(x + \alpha^2) \dots (x + \alpha^{2^t-1})$ $t = 0 - 10$ (programmable) FEC/Randomizer can be transposed in signal chain via control bus
I/Q Channel Invert	COS - j SIN or COS + j SIN, selectable via control bus
Preamble Insertion	0 - 96 bits, programmable length and content, enable/disable control, via control bus
Randomizer	Enable/disable control via control bus Generating polynomial: $x^6 + x^5 + 1$ with seed all 1's or $x^{15} + x^{14} + 1$, programmable seed Randomizer and FEC blocks can be transposed in signal chain, via control bus

*In FSK mode, F1:F2 are direct DDS Cosine output

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Table II. LEAD FUNCTION ASSIGNMENTS

Pin #	Pin Name	Pin Function
1	DGND	Digital ground
2	DVDD	Digital supply voltage
3	Control Bus Data Clock	Bit clock for bus control data
4	Bus Data In	Control bus control data in
5	FEC Enable	Enables/Disables FEC
6	Address Bit	Address bit for control bus
7	DGND	Digital ground
8	DVDD	Digital supply voltage
9	DGND	Digital ground
10	DGND	Digital ground
11	Test Data Out	Factory use - serial test data out
12	GND	Substrate ground connection
13	PLL GND	PLL ground connection
14	PLL VCC	Supply voltage for PLL
15	PLL Filter	PLL loop filter connection
16	AGND	Analog ground
17	N/C	No connect
18	DAC Rset	Rset resistor connection
19	AGND	Analog ground
20	AVDD	Analog supply voltage
21	DAC Baseline	DAC baseline voltage
22	AVDD	Analog supply voltage

Pin #	Pin Name	Pin Function
23	AGND	Analog ground
24	IOUT	Analog current output of the DAC
25	IOUTB	Complementary analog current output of the DAC
26	Test Data Out	Factory use - serial test data out
27	Test CLK	Factory use - scan clock
28	Test Latch	Factory use - scan latch
29	Test Data In	Factory use- serial test data in
30	Test Data Enable	Factory use - serial test data enable
31	Test Data Out	Factory use - serial test data out
32	RESET	Master device reset function
33	CA Enable	Cable ampl. enable
34	CA Clock	Cable ampl. serial control clock
35	CA Data	Cable ampl. serial control data
36	DGND	Digital ground
37	DVDD	Digital supply voltage
38	REF CLK IN	Reference Clock Input
39	DGND	Digital ground
40	DVDD	Digital supply voltage
41	Data In	Input serial data stream formatted as D1/D2/D3/D4...
42	Tx Enable	Pulse that frames the valid input data stream
43	DVDD	Digital supply voltage
44	DGND	Digital ground

Table III. Control Bus Register Functional Assignment (preliminary).Device I²C Address = 000001XX| ☐ Bidirectional mode: "1" = read/"0"=write| ☐ Pin 6 on device package set to "1" or "0" by user

Reg. Adr.	Register Function	Reg. Adr.	Register Function
0	8-bits, sets K value of RS encoder 0-255	24	8-bit FIR filter tap
1	(7 bits total) 4-bits, sets T value of RS encoder 0-10; value of 0 effectively disables/bypasses RS encoder	25	2-bit FIR filter tap
	1-bit, selects data path order between RS encoder and scrambler: 0=RS then scrambler, 1= scrambler then RS	26	8-bit FIR filter tap
	2-bits, selects length of scrambler: 00=6-bit length, 01=15-bit length, 10/11=disables scrambler,	27	2-bit FIR filter tap
2	15-bits total, sets seed value for scrambler, first 8 bits =MSB's	28	8-bit FIR filter tap
3	final 7 bits - LSB's		
4	7-bits, sets preamble length which matches the data delay after the RS/scrambler blocks. 96 bits max.	29	2-bit FIR filter tap
5	3-bits, modulation mode: 000=QPSK, 001=DQPSK, 010=16QAM, 011=D16QAM, 100=FSK	2A	8-bit FIR filter tap
6	8-bit preamble load byte, LSB	2B	2-bit FIR filter tap
7	8-bit preamble load byte NOTE:	2C	8-bit FIR filter tap
8	8-bit preamble load byte PREAMBLE IS LOADED FROM	2D	2-bit FIR filter tap
9	8-bit preamble load byte ADDRESS 11 TO 6. UNUSED	2E	8-bit FIR filter tap
A	8-bit preamble load byte ADDRESS BYTES OR BITS	2F	2-bit FIR filter tap
B	8-bit preamble load byte CAN BE IGNORED.	30	8-bit FIR filter tap
C	8-bit preamble load byte	31	2-bit FIR filter tap
D	8-bit preamble load byte	32	8-bit FIR filter tap
E	8-bit preamble load byte/additional ramp-up data	33	2-bit FIR filter tap
F	8-bit preamble load byte/additional ramp-up data	34	8-bit FIR filter tap
10	8-bit preamble load byte/additional ramp-up data	35	2-bit FIR filter tap
11	8-bit preamble load byte, includes ramp-up data, (recommended ramp-up data = all bits HIGH) MSB	36	8-bit FIR filter tap
12	5-bits, sets interpolation rate, S1	37	2-bit FIR filter tap
13	6-bits, sets interpolation rate, S2	38	8-bit FIR filter tap
14	6-bits, sets interpolation scaling, S1, first 5 bits (MSB's) set scaling, 6 th bit is a fixed multiply by 2 (1 = enabled, 0 = disabled)	39	2-bit FIR filter tap
15	6-bits, sets interpolation scaling, S2	3A	8-bit FIR filter tap
16	8-bit output frequency tuning word, bits 0-7	3B	2-bit FIR filter tap
17	8-bit output frequency tuning word, bits 8-15	3C	8-bit FIR filter tap
18	8-bit output frequency tuning word, bits 16-23	3D	2-bit FIR filter tap
19	8-bit output frequency tuning word, bits 24-31	3E	8-bit FIR filter tap
1A	8-bit F2 tuning word for FSK mode, bits 0-7	3F	2-bit FIR filter tap
1B	8-bit F2 tuning word for FSK mode, bits 8-15	40	8-bit FIR filter tap
1C	8-bit F2 tuning word for FSK mode, 16-23	41	2-bit FIR filter tap
1D	8-bit, F2 tuning word for FSK mode, bits 24-31	42	8-bit FIR filter tap
1E	8-bit FIR filter tap, END TAP	43	2-bit FIR filter tap
1F	2-bit FIR filter tap	44	8-bit FIR filter tap
20	8-bit FIR filter tap EIGHT LSB'S OF 10 BIT WORD	45	2-bit FIR filter tap
21	2-bit FIR filter tap TWO MSB'S OF 10 BIT WORD	46	8-bit FIR filter tap
22	8-bit FIR filter tap	47	2-bit FIR filter tap
23	2-bit FIR filter tap	48	5-bit, register for control functions, logic HIGH to enable, D7= 1/Q phase invert, D6 = Dig. Pwr Dwn, D5 = CLK multiplier enable/disable, D4 = CLK multiplier sleep mode, D3 = DAC sleep mode
		49	8-bits, sets gain of AD8320 cable driver amplifier

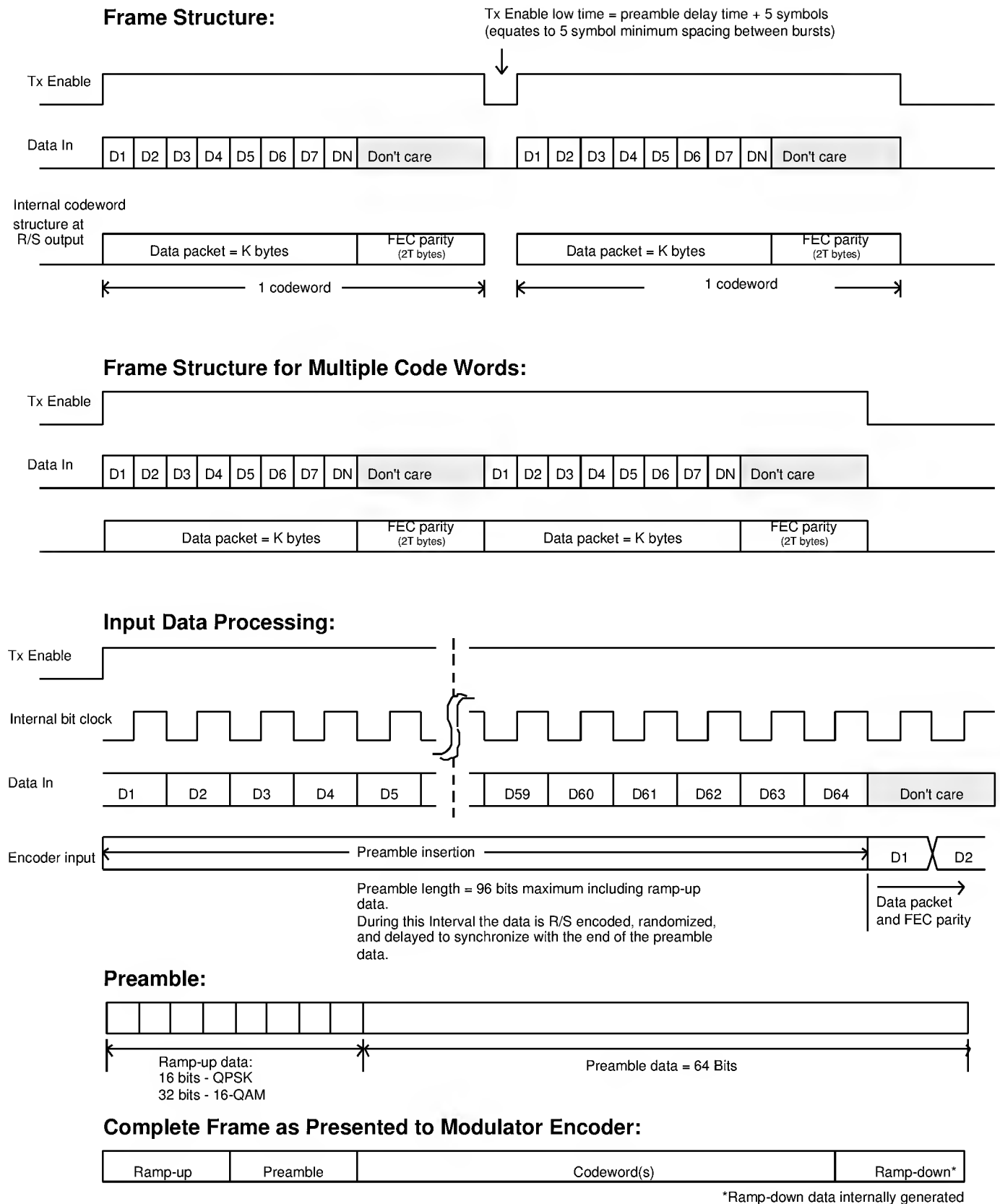
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Programming the interpolating filters

The function of the interpolating filter stage is to increase the effective sampling rate of the output data rate of the FIR filter stage, to exactly match the sine/cosine data clock rate at the digital mixer stage. The interpolation function is accomplished in two separate stages, S1 and S2. These individual interpolating stages are programmed via the control bus (see Table III for register addresses and functions). For optimal modulator performance, the total required interpolator multiplying factor to support a given input data rate, should be as equally spread as possible between the S1 and S2 stages. However, the lower of the two multiplication factors should always be implemented in the first stage. For instance, if the desired total interpolation rate is 32, set S1 for a factor of 4, and S2 for a factor of 8. The interpolator stage “scaling” values set the effective gain of the interpolating stage and, as a rule of thumb, generally set to 1 less than the interpolator multiplication factor. The scaling factor is set to yield the best observed spur performance (or other modulator performance criteria). If interpolator scaling is set too high, digital overflow can occur and results in gross signal distortion. If the scaling is set too low, loss of output amplitude will occur. Interpolator scaling values must be empirically set by measuring modulator operation.

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Figure 1. Burst Mode Timing and Interface



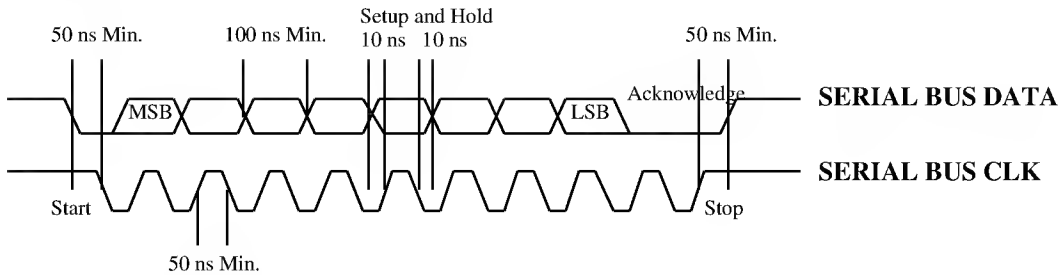
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Notes on Burst Mode Operation:

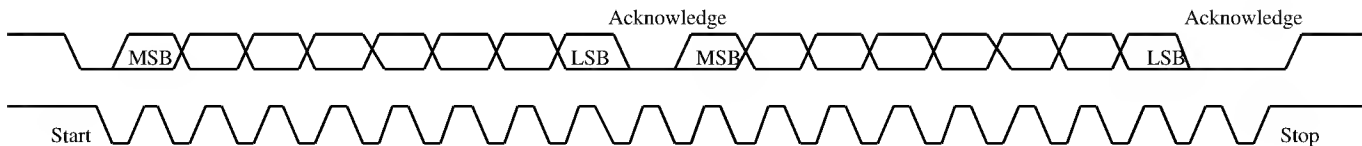
1. Packet length = number of information bits in codeword K
2. In FEC mode, Tx enable must be kept high for (K+2t) bytes for a 1 codeword burst, and (# of codewords X (K+2t) bytes) for multiple codeword burst
3. If necessary, zero fill the last codeword to reach assigned K data bytes per codeword
4. Data samples internally at $\frac{1}{2(\text{bit rate})}$ seconds, after rising edge of Tx Enable
5. Preamble delay = $\frac{1}{(\text{bit rate})}$ (# of preamble bits including ramp-up data)
6. 2 symbols (QPSK) = $(4) \frac{1}{(\text{bit rate})}$ 2 symbols (16-QAM) = $(8) \frac{1}{(\text{bit rate})}$

Figure 2. Serial Control Bus Interface Timing

Serial Bus transfer of 8 Data Bits



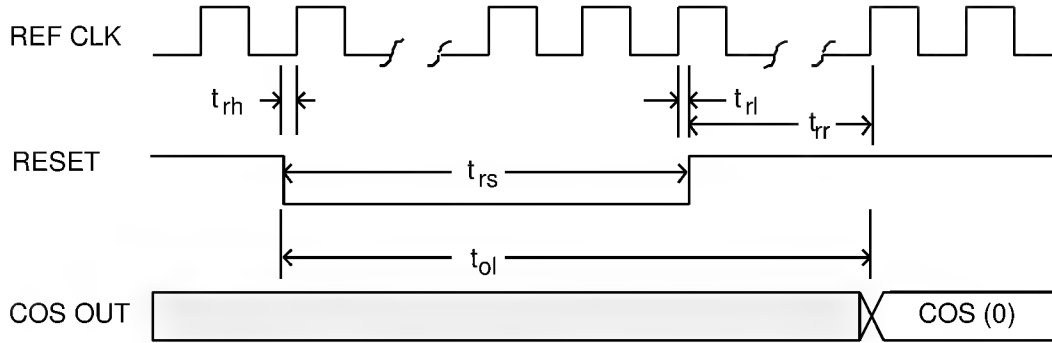
Serial Bus Transfer of Two 8-bit Words



Note: An 8-bit device address (000001X0) followed by an 8 bit control register address will allow the next 8 bits to be recognized as data for that register. When 8 bits of data have been transferred, the register address is automatically incremented and the next 8-bit data word for control register can be sent. If data are sequentially loaded, individual addressing of control bus registers is not needed after the first register has been addressed.

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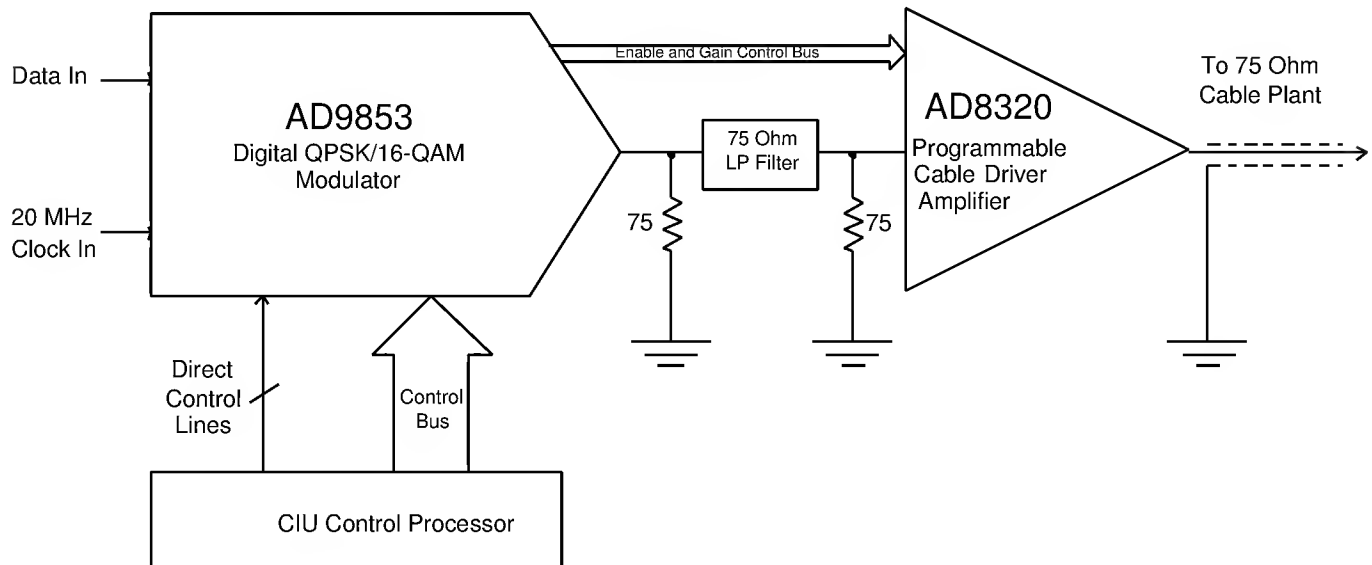
Figure 3. Master Reset Timing Diagram



Symbol	Definition	Min. Spec.
t_{rh}	CLK delay after Reset rising edge	3.5nS
t_{rl}	Reset falling edge after CLK	3.5nS
t_{rr}	Recovery from Reset	2 CLK cycles
t_{rs}	Minimum Reset width	5 CLK cycles
t_{ol}	Reset output latency	12 CLK cycles

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Figure 6. Basic Implementation of AD9853 Digital Modulator and AD8320 Programmable Cable Driver Amplifier in Return-path Application.



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Theory of Operation

The AD9853 is a highly integrated modulator function that has been specifically defined to meet the requirements of the HFC upstream function, for both inter-operable, and proprietary system implementations. The AD8320 is a companion cable driver amplifier, with a digitally-programmable gain function, that interfaces to the AD9853 modulator and directly drives the cable plant with the modulated carrier. Together, the AD9853 and AD8320 provide an easily implementable Tx solution for the HFC return-path requirement.

Data interface - As shown in the device's block diagram on page 1, the various burst profile parameters which include the input data rate, modulation format, FEC and randomizer configurations, as well as all the other modulator functions are programmed into the AD9853 via a 2-wire I²C-compatible bus. The AD8320 cable driver amp gain can be programmed directly from the AD9853 via a three wire bus by writing to the appropriate AD9853 register. The AD9853 also contains dedicated pins for FEC enable/disable and a master reset function.

The input data interface consists of two pins, the serial data input pin and a Tx Enable pin. The input data arrives at the bit-rate and is framed by the Tx Enable signal as shown in Figure 1. A high frequency sampling clock continuously samples the Tx Enable signal to detect the rising edge. Once the rising edge of Tx Enable is detected, an internal sampler strobes the serial data at the correct point in time relative to the positive Tx enable transition and then continues to sample at the correct interval based on the programmed Input Data rate.

Reed-Solomon Encoder - The sampled bit-rate data is then input to the first stage of the modulator system which consists of a Reed Solomon Forward Error correction circuit. A Reed Solomon (RS) code is a cyclic code consisting of a block sequence of Galois field symbols. A Galois field is a finite field consisting of 2^m elements. A particular Galois field of 2^m elements is defined by a primitive polynomial of degree m. A division algorithm between an element's location in the field and the primitive polynomial yields the element value. Each element is represented by m binary bits and corresponds to a codeword symbol. Both the encoding and decoding circuits in a communications system perform computations in the Galois field in order to realize the error correction function. The code being "cyclic" refers to the property that a cyclic shifting of a code symbol from the beginning of a code word to the end produces another codeword in the field. Cyclical codes reduce the complexity of the encoding and decoding process while maintaining good error correction properties. An (n,k) RS code generates a codeword with a maximum length equal to $2^m - 1$ bytes where m is the number of bits per symbol. The number of information symbols is denoted by k and the number of check symbols that is appended to the data symbols is equal to n-k. To generate the check symbols a division algorithm is performed in hardware between the k information symbols and a generator polynomial denoted as g(x). A corresponding FEC decoder makes use of the same generator polynomial at the receive side to decode and correct any symbol errors. The error correction capability of a given RS code is equal to $(n-k)/2$, usually denoted as t. The degree of the generator polynomial is equal to the number of parity check symbols, n - k. So from this a RS code is completely defined by the parameter m and the generator polynomial.

In the AD9853, n is programmable from 3 to 255 and T is programmable from 0 to 10.

Ideally, the highest transmit efficiency for a given n value is obtained when using little or no error correction as the ratio of information bytes to total bytes transmitted is highest. However as the noise environment dictates, the error correction capability can be increased at the expense of transmit efficiency or code rate.

Randomizer function - The next stage in the modulation chain is the randomizing or "scrambling" stage. Randomizing is necessary due to the fact that impairments in digital transmission can be a function of the statistics of the digital source. Receiver symbol synchronization is more easily maintained if the input sequence appears random or equi-probable. Long strings of 0's or 1's can cause a bit or symbol synchronizer to lose synchronization. If there are repetitive patterns in the data discrete spurs can be produced causing inter-channel interference. In modulation schemes relying on suppressed carrier transmission non-random data can increase the carrier feedthrough. Using a randomizer effectively "whitens" the data.

The technique used in the AD9853 to randomize the data is to perform a modulo 2 logic addition of the data with a pseudorandom sequence. The pseudorandom sequence is generated by a shift register of length m with an exclusive OR combination of the nth bit and the last (mth) bit of the shift register that is fed back to the shift register input. By choosing the appropriate feedback point a maximal length sequence is generated. The maximal length sequence will repeat after every 2^m clock cycles but appears effectively "random" at the output.

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The criterion for maximal length is that the polynomial $1+x^{**n}+x^{**m}$ be irreducible and prime over the Galois field. In the AD9853 there are two programmable polynomial values. The "seed" or initial register contents are also programmable.

Preamble insertion block - As shown in the block diagram of the AD9853 the circuit includes a programmable preamble insertion register. This register is 96 bits long and is transmitted upon receiving the Tx enable signal. It is transmitted without being Reed Solomon encoded or scrambled. Ramp up data to allow for receiver synchronization is included as the first bits in the preamble, followed by user burst profile or channel equalization information. The first bit of RS encoded and scrambled Information data is timed to immediately follow the last bit of preamble data.

Modulation encoder - The preamble, followed by the encoded and scrambled data is then modulation encoded according to the selected modulation format. The available modulation formats are FSK, QPSK, DQPSK, 16QAM, and 16DQAM. The corresponding symbol constellations support the emerging interactive HFC cable specifications called out by MCNS, 802.14 and DAVIC/DVB. The data arrives at the modulation encoder at the input bit rate and is demultiplexed as modulation encoded symbols into separate I and Q paths. For QPSK and DQPSK the symbol rate is one-half of the bit-rate and each symbol is comprised of two bits. For 16QAM and 16DQAM the symbol rate is one-fourth the bit rate and each symbol is comprised of four bits. In the FSK mode, although the 1 and 0 data is entered into the serial data input it effectively bypasses the encoding, scrambling and modulation paths and is routed directly to the direct digital synthesizer (DDS) where it is used to switch the DDS between two stored tuning words to achieve FSK modulation. In the FSK mode the modulator output is essentially a continuous wave that switched back and forth between the two stored frequencies in a phase-continuous manner. By holding the input at either 1 or 0, a single frequency continuous wave can be output for system test or CW transmission purposes.

Programmable pulse-shaping filters - The modulation encoded I and Q data then arrives at the programmable pulse shaping filters (square root raised cosine for MCNS) filters for baseband pulse shaping and filtering. Pulse shaping is necessary due to the finite bandwidth of the transmission channel and the tendency for un-shaped pulses to get spread in time so that they overlap adjacent pulses or symbols which gives rise to inter-symbol interference (ISI). ISI results in lower effective carrier-to-noise ratios (CNR) and increases the probability of bit-rate errors. To alleviate this problem pulses are shaped such that at a given sampling point, the Impulse response function's of all pulses prior to and after the current pulse are at zero. A class of filters which satisfy this requirement are known as Nyquist filters. In practice these filters are defined with an excess bandwidth term denoted as alpha which defines the additional bandwidth required over the Nyquist bandwidth, which is $1/2T$ where T is the symbol length in time. If the filter bandwidth is constrained to the Nyquist bandwidth, the slopes of the impulse function response at the symbol interval zero crossing point are relatively steep and the constraints on the timing accuracy are more severe as small errors in timing will result in "missed" zero sampling, resulting in ISI. Using a higher alpha filter will sacrifice bandwidth but the slopes of the impulse functions as they cross zero are not as steep, so small timing errors can be tolerated without producing severe ISI.

The AD9853 uses 41 tap programmable Fir filters for the SRRC filters. The filter taps are 10 bits in length which will provide the required shaping and bandwidth containment performance required for cable data systems. These filters are typically matched to corresponding receive side SRRC filters which when convolved with one another, produce a raised cosine filter response. Each symbol is over-sampled by four which produces an effective sample rate at the output of the Fir filters of 4X the symbol rate.

Programmable interpolating filters - After to the pulse shaping filter stage, interpolation filters are used to effectively up-sample the signal to the system clock rate while attenuating aliased components down to acceptable levels. The interpolators must also provide a passband with a negligible impact on the baseband spectrum. To accommodate a wide range of data rates the interpolation ratio in the AD9853 is programmable from 4 to 2048. The gain of the interpolation filters is programmable as well, to provide a means of spectral optimization for given data rates. It should be noted here that since the I and Q modulation filter chains are fully digital, they are matched exactly in terms of their phase and gain properties and are immune to channel coupling effects, which can be a problem in analog implementations.

Mixers, adder, inverse sinc functions - At the output of the Interpolation filters, the pulse-shaped, up-sampled I and Q baseband data is multiplied with digitized quadrature versions of the carrier, $\cos w_c t$ and $\sin w_c t$ respectively, which are provided by a direct digital synthesizer (DDS) block. The DDS block has a 32 bit tuning word which results in an extremely fine carrier frequency tuning resolution of $F_{\text{clock}}/2^{**n}$ as well as extremely fast frequency switching. The multiplier outputs are then summed, to form the QPSK/QAM modulated signal. This signal is then filtered by an inverse sinc filter to compensate for the $\sin X/X$ rolloff function inherent in the sampling process of digital-to-analog conversion. The inverse sinc filter flattens the gain response across the Nyquist bandwidth.

AD9853 PRELIMINARY INFORMATION

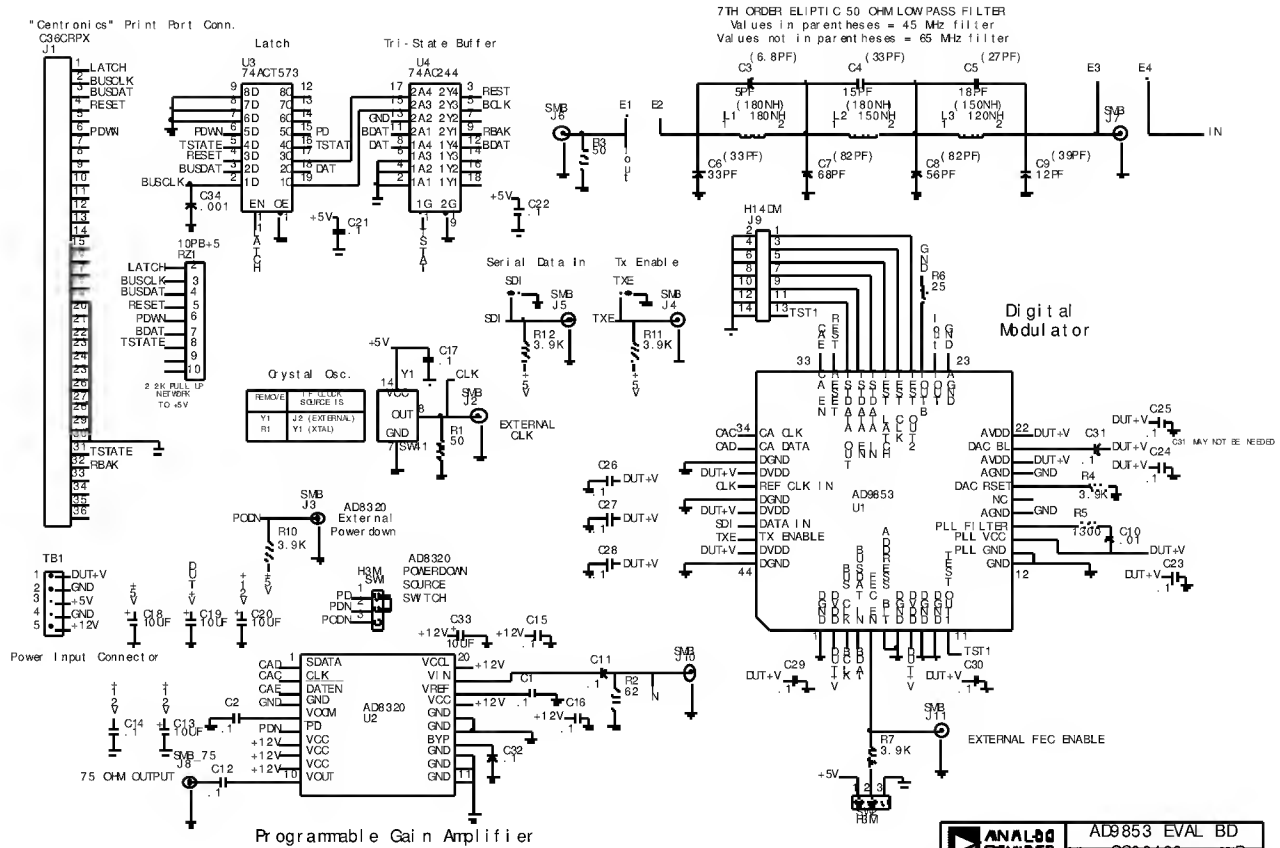
This is most critical for higher data rate signals that are placed on carriers at the high end of the spectrum where the uncompensated $\sin x/x$ rolloff would be getting progressively steeper. Gain attenuation across a channel will result in modulation quality impairments, such as degraded error vector magnitude (EVM).

D/A converter - Up to this point all the processing has been in the digital domain. In order to pass the modulated signal onto the cable driver for amplification to the levels required to drive the 75 ohm cable, a digital-to-analog converter (DAC) is implemented. The DAC needs to have good enough transient characteristics so as not to add significant spurious in the spectrum. Typically the worst spurs from the DAC are due to harmonics of the fundamental signal that fall in-band either naturally or from out-of-band aliases. These harmonics are worst case for the higher carrier frequencies. Design improvements in CMOS DAC's have reached the point where better than -50dbc spurious can be maintained across the 5-42MHz spectrum with significantly better performance (-60 dBc) at lower carrier frequencies. The conversion process will produce aliased components at the DAC output at $nF_{\text{clock}} \pm F_{\text{carrier}}$. These are typically filtered with an external RLC filter between the DAC and the line driver amplifier. Again, it is important for this analog filter to have a sufficiently flat gain and linear phase response across the bandwidth of interest so as to avoid the aforementioned modulation impairments. A relatively inexpensive 7 pole-elliptical low-pass filter is sufficient to suppress the aliased components for HFC network applications.

Reference clock multiplier - Due to the fact that the AD9853 is a DDS-based modulator, a relatively high frequency system clock is required. For DDS applications the carrier is typically limited to about 0.4 percent of F_{clock} . For a 65 MHz carrier, the system clock required is above 150 MHz. To avoid the cost associated with these high frequency references, and the aggravating noise coupling issues associated with operating a high frequency clock on a PC board, the AD9853 provides an on-chip 6X clock multiplier. With the 6X on-chip multiplier, the input reference clock required for the AD9853 can be kept in the 20 to 30MHz range which results in cost and system implementation savings. The 6X on-chip multiplier maintains clock integrity as evidenced by the AD9853's system phase noise characteristics of -100 dBc/Hz and virtually no clock related spurious in the output spectrum.

AD9853 PRELIMINARY INFORMATION

Figure 5. Schematic diagram of AD9853 evaluation board.



	AD9853 EVAL BD	
	REV B	CS00466
6/23/97	R. Cushing	B. Podd/T. Hecht

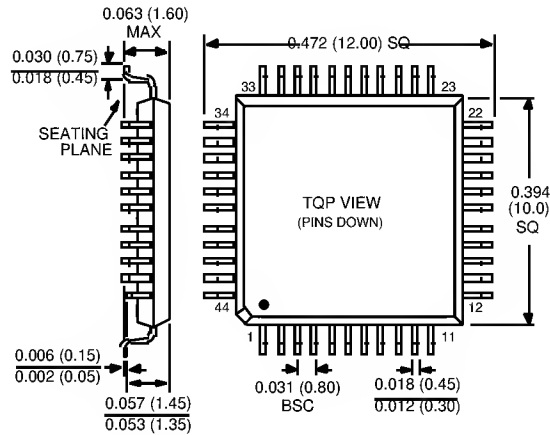
AD9853 PRELIMINARY INFORMATION

Application Note: 5-65 MHz Analog Output Operation

5-65 MHz Aout operation is achieved with the AD9853 under the conditions of an internal clock speed of 162 MHz (external Ref. Clock = 27 MHz), and +5 V supply voltage.

**Figure 6. Mechanical Outline
44-Lead Metric Quad Flatpack IC Package (MQFP)**

SUBJECT TO CHANGE



For further information on the AD9853 contact:

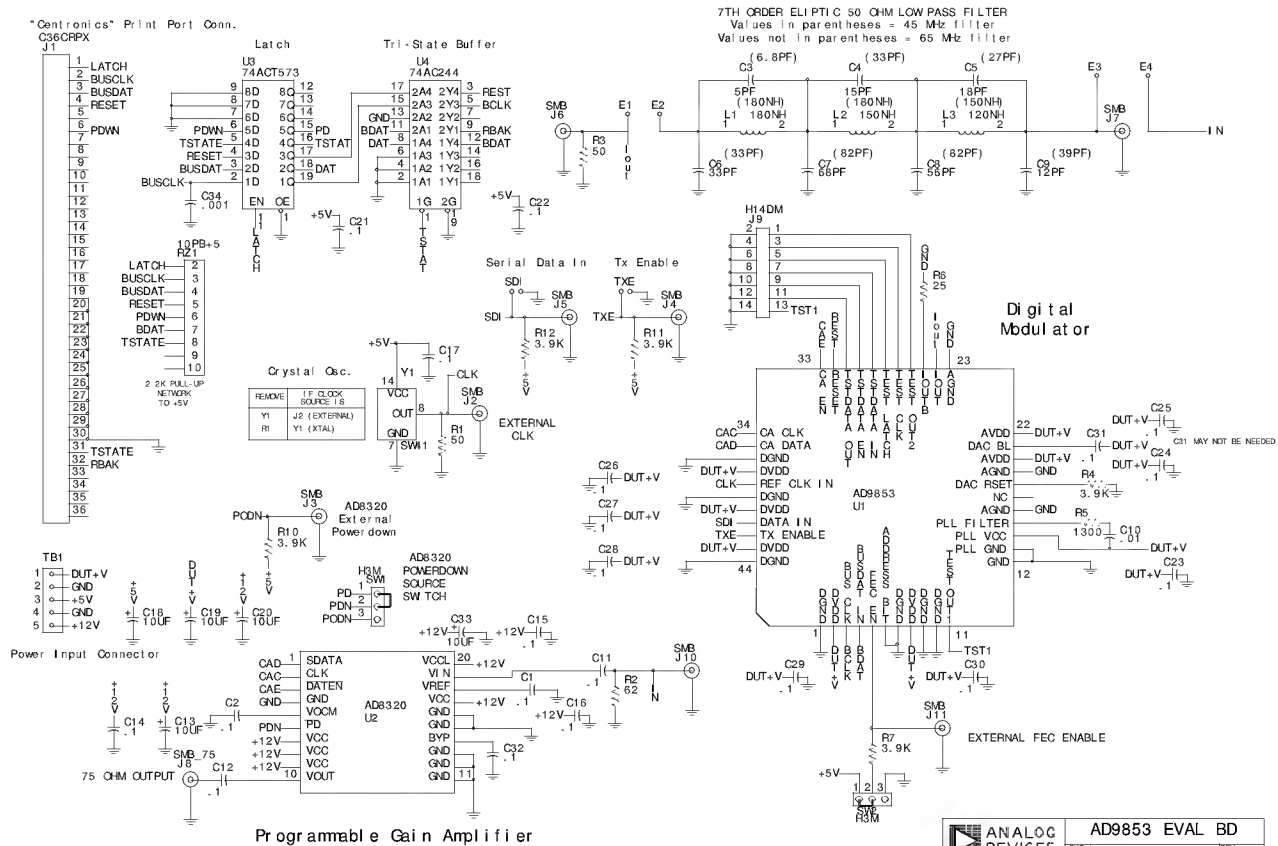
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AD9853 PRELIMINARY INFORMATION

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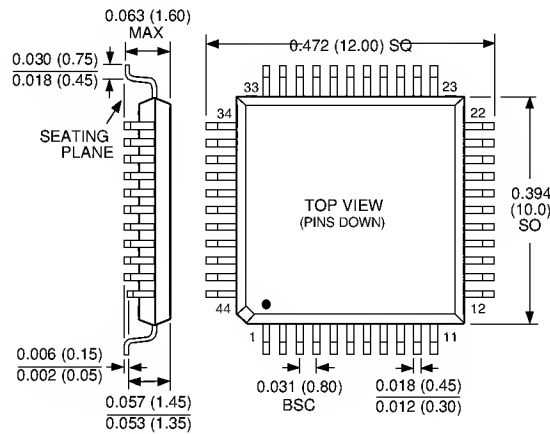
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